Quarterly Newsletter

Spring 2020

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Introduction

These are trying times for everyone! Since APEC was cancelled due to the Corona virus, we understand now just how close we were to disaster. Little did we know at the time that the virus was spreading like wildfire in New Orleans during the week following Mardi Gras in which the conference was scheduled. Had the show proceeded, more than 5000 attendees from all over the world could have been exposed and carried the infection back to their homes around the globe. How much worse could the pandemic have been had we contributed to the spread?

The APEC committee experienced serious angst and was under much pressure to make the right call. In retrospect we know that cancelling the show probably saved lives and was the correct decision. So, let's all give a salute and commend the APEC committee as we look forward to APEC2021 in Phoenix next March 21-25!

Working Group Updates

While disappointed that we had to cancel our Spring 2020 face to face meeting at APEC 2020, the PMBus Specification Work Group continues to meet weekly to discuss topics on improving the PMBus Specification.

The Specification Work Group has completed their review of typos and clarifications in the SMBus Specification 3.1 based on user feedback submitted to the SMIF help line and submitted Revision 3.2 to the SMIF board of directors for review.

As agreed upon last year, the PMBus Specification Work Group has been working hard to prepare Revision 1.4 for membership voting. Part I and Part III changes appear to be complete while final discussions and edits in Part II are still on-going.

Revision 1.4 will include clarifications, and a minor change to the PAGE_PLUS_READ and PAGE_PLUS_WRITE commands as well as adding the PHASE_PLUS_READ and PHASE_PLUS_WRITE commands to allow the reading from or writing to specific phases within specific pages on a device.

With the conclusion of the Work Group's review of Revision 1.4, the we are looking to the future of digital power management and the development of PMBus 2.0.

The Specification Work Group has also restarted the Standard Configuration File Format sub-group to define a SMIF endorsed standard file format for defining the configuration programming of PMBus compatible devices that can be shared across vendors in order to easy the adoption of in-

circuit programming of multi-vendor Power Systems using PMBus.

If you have questions or would like to contribute, please contact the leader of the working groups, Peter Miller of Texas Instruments at peter_miller@ti.com.

Membership Updates

As mentioned in the last newsletter, there has been a flurry of acquisition activity amongst our member companies. When a PMBus member company acquires or merges with another company who is also a member, the two separate memberships 'merge' under the parent company, thus reducing our member count by one. Several companies that had never offered PMBus products have scuttled their future development plans and decline to renew membership.

The present membership count is 38, comprising 35 full members and 3 tools members. You can refer to the *PMBus adopters* page of our website for the full details and benefits of membership.

Interested in joining PMBus? Get a detailed description of the System Management Interface Forum and membership benefits by clicking PMBus Organization Overview. Or, just send an email to admin@smiforum.org to get immediate answers to specific questions.

New Product Announcements

Infineon's REF_600W_FBFB_XDPP1100 reference design is a system solution for telecom isolated dc-dc power modules that achieves 96% peak efficiency in a DOSA standard quarter brick form factor. This reference design introduces a secondary side digital control and hard switching full-bridge topology delivering 12V/600W of output power. It operates across a wide range of input voltages (36V to 72V). The achieved power density is 22W/cm³ (360 W/in³), which is enabled by the use of the XDPP1100 digital controller, OptiMOS™ MOSFETs and an EiceDRIVER™ gate driver IC.

The XDPP1100 digital power supply controller IC with PMBus and I2C communication includes an optimized analog front end, multiple pre-programmed peripherals, a fast state-machine based control loop, and a microcontroller. This unique architecture enhances the performance of isolated dc-dc applications, reduces BOM size, and allows advanced control functions as well as customization, while providing the fastest time to market.

Maxim Integrated Products new MAX16545B/C is a circuit-breaker protection IC with an integrated low-resistance MOSFET and lossless current-sense circuitry featuring PMBus®/SMBus telemetry with extensive status monitoring and reporting. The IC is designed to provide the optimum solution for distribution, control, monitoring and protection of the system's 12V power supply. An internal LDO provides the bias supply voltage for the protection IC.

The IC monitors the current and the voltage of the 12V system power rail and provides multiple levels of protection with fast turn off if a fault is detected. Three methods of overcurrent protection are provided. Programmable moderate OCP level allows surge currents for a limited time. User-selectable severe OCP level provides a fast disconnect if a current exceeding the severe OCP threshold is detected. An additional fixed high shutdown OCP level provides instantaneous disconnect to further protect the device.

Monolithic Power Systems new MP4245 is a buck-boost converter with 4 integrated power switches in a QFN21 (4mm x 5mm) package . The device can deliver up to 6A output current at certain input-supply range with excellent load and line regulation.

The MP4245 is suitable for USB power delivery (USB PD) applications. The MTP (2 times programmable) and I2C interface with PMBus compatibility provide flexibility of programmable features. Fault condition protection includes CC current limiting, output OVP, and thermal shutdown (TSD).

Monolithic Power Systems released the MPM82504, a quad 25A, scalable and fully integrated dc-dc converter with PMBus interface. MPM82504 offers a complete power solution that achieves up to 25A per output channel. Four output channels of MPM82504 can be connected in parallel to provide 50A, 75A, or 100A output current.

MPM82504 adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control, which provides ultra-fast transient response and simple loop compensation. IT features full protection functions including over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP). A PMBus interface provides module configurations and monitoring of key parameters.

NXP The fully digital design of the KV46 digital LLC dc-dc converter reference design is based on NXP‘s HVP-LLC development board. The HVP-LLC dev board is an integral part of NXP high-voltage platform. In combination with the HVP-KV46F150 controller card, it provides a ready-made software development platform for 250W LLC dc-dc converter with an input voltage of 390Vdc and a 12V / 21A output.

This dc-dc converter design includes GaN power FETs and synchronous rectification, plus analog sensing (resonant tank current, output voltage, output current). It has a PMBus communications interface and over current protection on both the input and output.

Texas Instruments (TI) introduced a new 40-A SWIFT™ dc-dc buck converter, offering first-of-its-kind stackability of up to four integrated circuits (ICs). The TPS546D24A PMBus buck converter can deliver up to 160A of output current at an 85°C ambient temperature. The small size (5x7mm, 40-pin QFN package) and low thermal resistance (8.1°C/W) address two key considerations for engineers designing power supplies for modern FPGAs.

The TPS546D24A offers a switching frequency of 1.5MHz and features a 0.9mΩ low-side MOSFET to improve efficiency. Offering an output voltage error of less than 1%, it comes with a PMBus interface a selectable internal compensation network, allowing engineers to monitor current more accurately for fault reporting and to avoid overdesign.

Vicor has announced the DCM5614, an isolated, regulated 270V-to-28V dc-dc converter with an output power rating of 1300W in a 5.6 x 1.4 x 0.3 inch VIA™ package. Providing unmatched power density of 451W/in3 at a weight of just 178g, the DCM5614 supports advanced airborne, shipboard and UAV systems where power density, weight and efficiency are critical. Modules can also be easily paralleled for increased power or stacked for increased output voltage

The DCM's 96% efficiency and innovative planar and thermally adept VIA package enables multiple cooling strategies for enhanced thermal performance. It offers low noise, fast transient response and high power density. The optional secondary referenced PMBus-compatible telemetry and control interface provides access to the DCM's internal controller configuration, fault monitoring and other telemetry functions.

If your company has new products that you would like to be included in our next newsletter, just send an email with the subject line "new product(s)" and the details to admin@smiforum.org. Then watch this space for updates.

Website Updates

Even through the pandemic our members continue to release PMBus-compliant products. Currently there are 475 items displayed on the *Products* pages of the PMBus website. Include are semiconductors and power supplies as well as other supporting material such as application notes, evaluation kits, articles, reference designs, and videos.

The dedicated *Products* pages are one of the benefits of PMBus membership. They enable our members to identify and promote all of their PMBus-compliant products. We encourage you to contact us when you are ready to include or update your company's product listings.

You can click here to see an example of the Texas Instruments *Products* page. Be sure to utilize the "Featured Product", option which includes graphics on your company's page. Please send any request for changes to admin@simforum.org

New Website.
The new PMBus website is being finalized and tested. Launch is expected later this summer. In addition to a new 'look & feel', the site will include simplified usability for content updates and an integrated contact database for subscription and email. For the 2600+ of you on our mailing list , you will receive an email notification as soon as the new website is launched.

Promotional Activities

We invite you to join the PMBus Group on LinkedIn. In the future we will be utilizing the platform for new product announcements, meeting notifications and other newsworthy items.

Upcoming Events

Mark your calendars to visit the PMBus booth at the upcoming **APEC 2021 Conference & Expo** at the Phoenix Convention Center in Arizona March 21-25. This year Artesyn will be demonstrating their PMBus communications over an ethernet link to remotely control a power supply back at their laboratory in Arizona.

FAQ

This newsletter's *Frequently Asked Question* section includes multiple inquiries about AVSBus data transmissions.

Can you please help clarify a few questions regarding AVSBus. I am referring to "PMBus_Specification_Part_III – AVSBus Revision 1.3.1"

Question 1: *Can the Master transmit a <StartCode> right away when the Clock starts (shown in figure 1 below)? Section "5.2 Operation" mentions "AVS_MData is not allowed to be at a logic value '0' when the clock starts". Does this mean the first bit transmitted after a Clock starts must be a "1". Is the Master's behavior in the figure below incorrect?*

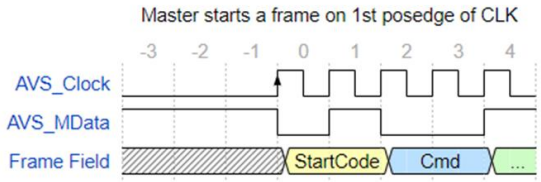

Figure 1

Answer 1: AVS_MData is not allowed to be at a logic value '0' when the clock starts is consistent with "the slave must keep the line high when the clock is suspended (Found in section 5.5).

Considering that the master launches data on the rising edge, that <StartCode> 01 really begins after the rising clock edge. This does not violate the condition above, since AVS_MData would be at logic value '1' since before the rising edge of the clock until soon after the rising edge when it changes to '0' (when that condition no longer applies).

So, Figure 1 is correct and the first bit transmitted after a Clock starts may be a "0" or "1".

Question 2: *Per Section 6, data is launched on the rising edge and sampled on the falling edge of Clock.*

Consider the case where last bit of slave frame is "0". If the Master suspends the clock immediately upon sampling the last bit, then the AVS_SData will be stuck at "0" (see figure 2 below).
Therefore, the Master must drive one more CLK pulse so that the slave can complete the

frame transmission. This will allow the slave to drive idle ("1") on the AVS_SData bus.

Is my understanding correct? Also, Is there a recommendation on what are the ideal conditions for the Master to suspend the CLK?

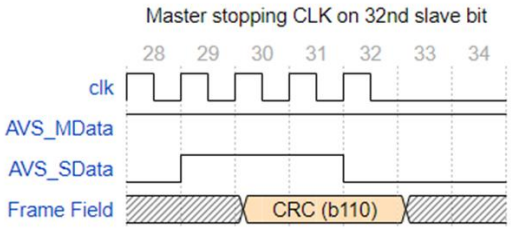

Figure 2

Answer 2: Consider the case where last bit of slave frame is "0". If the Master suspends the clock immediately upon sampling the last bit, then the AVS_SData will be stuck at "0".

The master is free to suspend the clock between sequences of frames--but not at other points in time--because suspending the clock between frames in a sequence can lead to the situation depicted in the image submitted with the question. In fact, the same happens if the master suspends the clock arbitrarily in the middle of a frame at the moment that the slave is sending a logic '0'.

Section 7.3 describes how the master would send frames back to back for as long as there is information to send/receive, but end the sequence with an "All 1's" subframe that would mark the point at which the interface can go idle. That being said, it is possible for the last bit of the <CRC> in AVS_SData to be '0', and a well-behaved master would send one more "All 1's" subframe.

Therefore, the Master must drive one more CLK pulse so that the slave can complete the frame transmission.
Nothing prevents the Master from sending just one more clock period while holding AVS_MData at '1' in that specific situation, or right after every sequence of frames. After all, there is no requirement that there would be zero clock idle periods between sequences of frames (that is just an option for saving power and reducing noise) , nor that the number of idle clock periods be a multiple of 32.

Have a question about the PMBus or SMBus specifications? SMIF technical volunteers provide free answers. Send your question to techquestions@smiforum.org and a PMBus or SMBus consultant will respond.

Other Items

The PMBus name and logo are registered trademarks of SMIF. PMBus adopters who are SMIF members in good standing are allowed free, unlimited commercial use of the PMBus name and logo. Proper usage of the name and logo is important in order to retain our rights. Please encourage your company's marketing communications department to collaborate with SMIF whenever there are publications or questions.

Please remember to use the ® symbol when referencing PMBus and the ™ symbol with AVSBus in data sheets, press releases or other written material. It should be included in any title or blurb and with the first usage in the main text for articles. The logo graphics for web postings and hi-res print can be downloaded from the resources section of the PMBus website.

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